



# ICA-XFG-101

## Introduction to P4<sub>16</sub>, Intel® Tofino™ Family and Intel P4 Studio™ SDE

### Course Prospectus

ICA-XFG-101 is 6-unit introductory, instructor-led course module that provides a quick, hands-on introduction to the basics of P4<sub>16</sub> language and a simple Intel® P4 Studio SDE development workflow. This course is recommended to anyone who wants to start learning P4 and Intel® P4 Studio and is a required pre-requisite for other online courses.

ICA-XFG-101 is a part of Intel® Connectivity Academy XFG course series and can be taken either in-person or online.

### Course Goals

Upon the completion of the course, the students will:

1. Learn the foundations of P4<sub>16</sub> language and Tofino Native architecture (TNA)
2. Learn how to write simple P4<sub>16</sub>/TNA programs, compile and run them both in on the model and on the real device
3. Understand the architecture of the P4 Studio SDE software stack and learn how to compile and build it, both for VM and ASIC Environment
4. Understand the basics of Tofino processing pipeline and learn the basics of using P4Insight™ tool
5. Learn the basics of Barefoot Runtime Interface (BRI) and several forms of its Python bindings
6. Learn the foundations of Packet Test Framework (PTF) and how to write PTF tests
7. Learn several methods of P4 program debugging using both the model and the real hardware
8. Understand where and how to get help and support in various scenarios
9. Get prepared to take Level2 courses

## Detailed Schedule

Each unit consists of a 2-hour-long lecture (presentation) with one break and is followed by the hands-on labs.

In online format, each unit is conducted on a separate day – please consult the Academy Calendar for details. Both morning and evening (Pacific Time) sessions are offered to accommodate students from different time zones.

When conducted in-person, each 8-hour day constitutes 2 units.

### Unit 1: Introduction and the first program

- Introduction
- P416: Data Plane Model (PISA)
- P416: Language Elements
- P416/TNA: A simple Example
- P4 Studio™ SDE: A Basic P4 Workflow

### Unit 2: P4 Studio SDE

- P4 Studio SDE Distribution Structure, Components and Architecture
- Board Support Package (BSP)
- SDE build and Installation
- Building and Visualizing P4 Programs
- Getting Help and Support

### Unit 3: TNA Showcase

- Parsing complex packets
- Arithmetic in P4
- Counter and meter basics
- Hash calculations
- Action profiles and action selectors
- Multicasting
- Mirroring
- Multi-pipe programming

### Unit 4: Barefoot Runtime Interface and Packet Test Framework

- Barefoot Runtime Interface basics. BfRt and BF Runtime
- API bindings
- Simple template for the BF Runtime control plane application
- Packet Test Framework architecture
- Writing simple PTF tests

### Unit 5: Tofino™ ASIC Family Architecture

- Device Overview

- Port Interfaces
- Unified Match-Action Pipeline architecture
- Programmable Header and Metadata Bus (Packet Header Vector)
- Programmable Parser
- Programmable Match-Action Pipeline and its resources
- Programmable Deparser

#### Unit 6: Running and Debugging P4 programs

- Using Wedge-100B system
- Using engineering CLI (ucli)
- Programmatic port management using BRI
- Running standard diagnostics (bf-diags)
- Debugging with counters
- Debugging with snapshots
- Conclusion

### Target Audience

This course is most suitable for designers and architects, tasked with design and development of data plane and control plane programs for modern networking equipment.

### Pre-requisites

- General understanding of network and telecommunications architecture and protocols
- Understanding of C and C++ languages, especially as it relates to embedded and NOS development
- Knowledge of Python language
- Experience in data or control plane design is extremely helpful
- When taken online, good and reliable Internet access for both online lectures and VM access is a must
- When taken in-person, each participant is expected to have a laptop with a standard browser. No other software is required

## How to Register

Class dates and times are announced on the [Academy Calendar Page](#) ahead of time and you can register right on the site using the credit card or PayPal to pay for the tickets. The tickets can also be purchased via standard sales channels. Please, contact your Intel sales representative for more details.

Please, note that most courses require all the participants to have a valid NDA and SLA in place. Their existence will be verified after the purchase, and you will be notified if additional steps are required, or the ticket will be refunded.

## Logistics

### Online courses

To attend an online presentation, you will need to create a **free Zoom account, associated with your work email address**. Upon the registration, you will receive a link to the online event. You will also receive invitations to establish accounts on Slack and the [Academy Support Portal](#) for lab support and materials access, also **associated with your work email address**.

A high-speed internet connection is required to attend the online presentation. Call-in numbers for higher voice quality might be provided, depending on the region. Please, connect to the online meeting 5-10 minutes before the start to work out all potential connection problems.

All necessary materials, including the presentation PDFs and lab exercises will be available through the [Academy Support Portal](#) a day before the start of the class. We highly recommend that you print the presentation PDFs and use them to take notes. Alternatively, these presentations can be loaded on a tablet, where the notes can be taken with an electronic pen.

The information about the lab Virtual Machines will be provided at the end of the first lecture. VMs will be kept running throughout the duration of the course and shut down 48 hours after the end of the last class. Additional time can be purchased as a ticket add-on.

### In-person courses

The location address and the arrival time can be found on the registration site and will be emailed to you as well. You are responsible for your own lodging and transportation; Academy staff will be happy to provide some recommendations.

You will receive invitations to establish accounts on Slack and the [Academy Support Portal](#) for lab support and materials access, also **associated with your work email address**.

All necessary materials will be printed for you and are yours to take notes and take them back home. You will also get a lifetime access to the updated versions of these materials on the Academy Support Portal.

The information about the lab Virtual Machines will be provided at the end of the lecture. VMs will be kept running throughout the duration of the course and shut down 48 hours after the end of the last class. Additional time can be purchased as a ticket add-on.

## Contact

For more information, please contact [connectivity.academy@intel.com](mailto:connectivity.academy@intel.com).

## Important Notes

Intel® P4 Studio SDE is a software product, developed independently from the software, available via p4.org. Some components of the SDE were contributed by Intel to p4.org, others rely on the code from p4.org, but the goals of the projects, the tools, and the workflows are different. P4.org software is a community-supported project with many resources freely available. This class covers Intel® P4 Studio SDE and **not** p4.org software. Specifically, not covered are the Behavioral Model (BMv2), v1model and PSA P4<sub>16</sub> architectures and neither is P4Runtime protocol.

P4<sub>16</sub> compiler for Intel® Tofino™ and Intel® Switch Runtime Interface APIs are in active development as is the course module material. While Intel® Connectivity Academy team strives to introduce Intel customers to the leading-edge software, bugs, errors and omissions may occur. The later versions of these course modules might significantly differ from the earlier ones.

The course module material covers both Tofino and Tofino2 devices. Relevant enhancements and differences are emphasized and discussed whenever applicable.

The availability of each course is announced separately. Please, visit [Intel® Connectivity Academy](https://www.intel.com/content/www/us/en/programmable/development-hub/connectivity-academy.html) website for more information.

The online presentations may be recorded and may be published, in whole or in part, in various media, including print, audio and video formats without further notice. If you do not want to participate, you may choose to either keep your audio and video connections muted or turned off or leave the call. By choosing to remain, you are consenting to the recording of the session.