OSFP 800Gbps (2x400Gbps) Optical Transceiver

T-OL8CNT-N00

Product Specification

Preliminary

Features

- OSFP MSA Compliant
- CMIS 4.0 Fully Compliant
- 2 sets of 4 CWDM lanes MUX/DEMUX design
- Electrical interface: compliant with 800GAUI-8 (8x106.25Gb/s) interface defined in IEEE 802.3ck
- Up to 3km transmission on single mode fiber (SMF) with KP4 FEC support at the host
- Operating case temperature: 0 to 70°C
- Rate Date operation at 106.25Gbps (PAM4) per channel
- Maximum power consumption less than 16W
- Dual Dual duplex LC connectors
- RoHS compliant

Applications

- Data Center Interconnect
- 800G Ethernet
- InfiniBand interconnects
- Enterprise networking

Part Number Ordering Information

T-OL8CNT-N00	OSFP 2x400G FR4 optical transceiver with full real-time digital diagnostic monitoring and pull tab

1. General Description

This product is a transceiver module designed for 3km optical communication applications. The design is compliant to IEEE 802.3ck Specification. The module converts 8 input channels of 106.25Gb/s electrical data to 2 sets of 4 CWDM optical signals and multiplexes them into 2 sets of a single channel for 425Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes 2 sets of a single channel 425Gb/s signal inputs into 2 sets of 4 CWDM channel signals and converts them to 8 output channels of 106.25Gb/s electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains an optical Dual duplex LC connector for the optical interface and a 60-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2km fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the OSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

2. Functional Description

The module incorporates 2 sets of 4 independent Channels, on CWDM4 1271/1291/1311/1331nm center wavelength, operating at 106.25Gb/s for each channel. The transmit path of the module incorporates a bi-directional PAM4 retimer ASIC integrated with an 8-channel modulator driver, 8 externally modulated lasers (two on each CWDM channel) and two optical multiplexers. On the receive path, two optical demultiplexers are coupled to 8 photodiodes and two 4-channel TIA arrays, along with the PAM4 retimer. The electrical interface is compliant with IEEE 802.3bs and OSFP MSA in the transmitting and receiving directions, and the optical interface is compliant with Dual duplex LC optical connectors. Figure 2 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. As per MSA specifications the module offers 4 low speed hardware control pins: SCL, SDA, INT/RSTn and LPWn/PRSn

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value can be 2.2k ohms to 4.7k ohms.

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host. The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 1 shows these 3 zones.

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host. The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 1 shows these 3 zones.

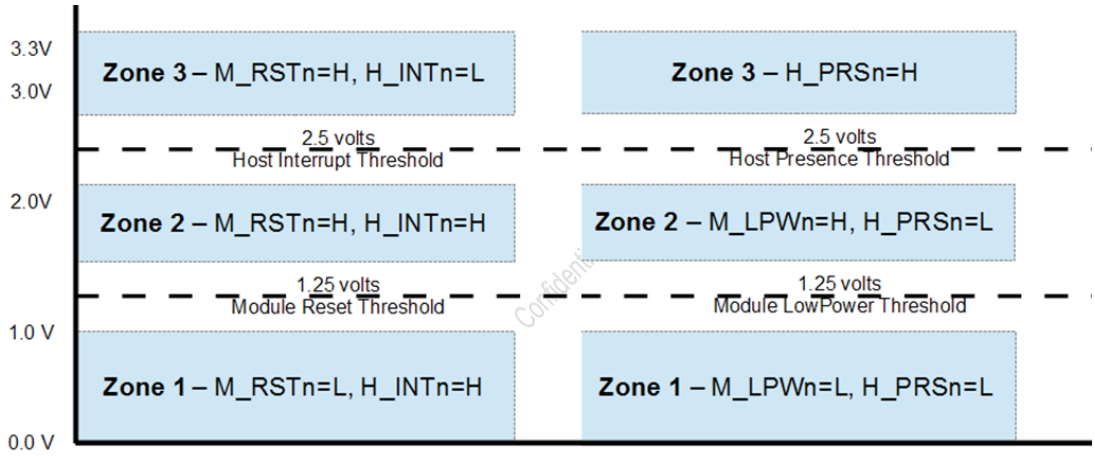

Figure 1. Voltage Zones

3. Transceiver Block Diagram

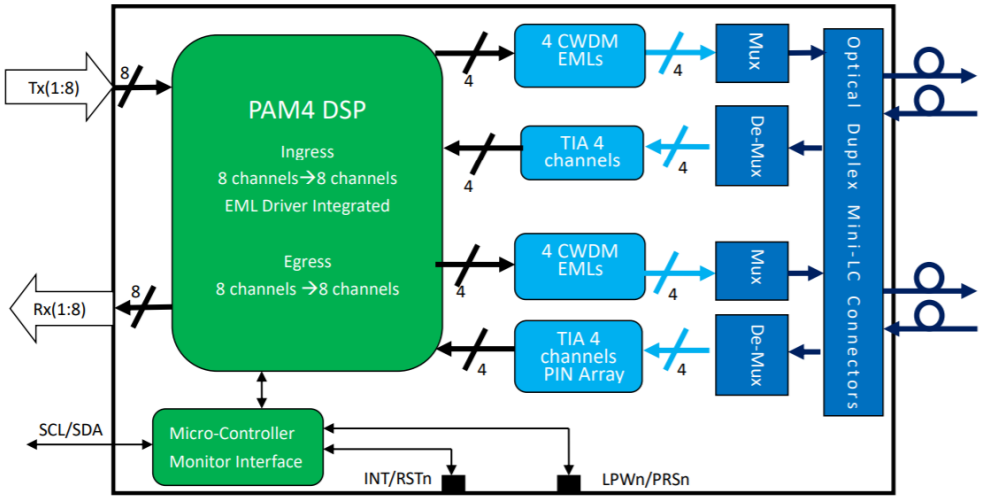

Figure 2. Transceiver Block Diagram

4. Pin Assignment and Description

The electrical pinout of the OSFP module is shown in Figure 3 below. Table 1 shows the electrical to optical channel mapping scheme.

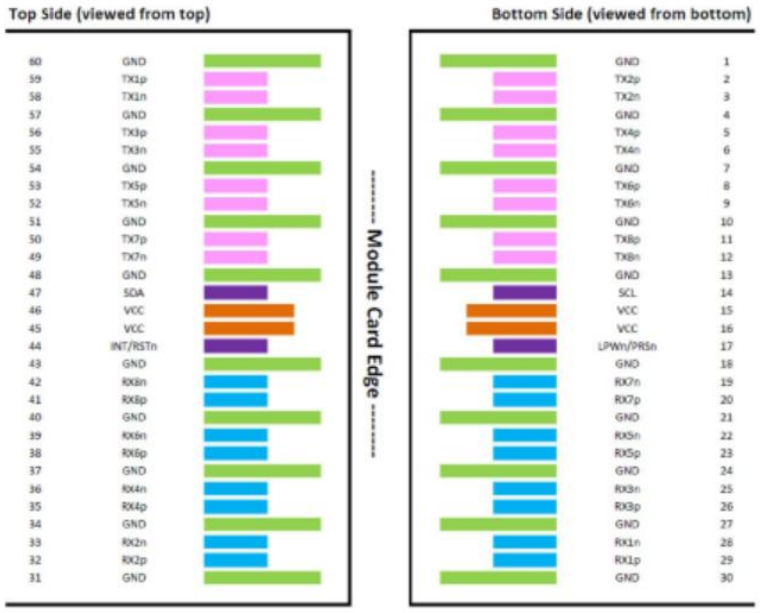

Figure 3. MSA compliant Connector

Pin Definition

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3

30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Table 1. Electrical to Optical Channel Mapping

Electrical Channels	Optical Wavelength (nm)
1	1270
2	1290
3	1310
4	1330
5	1270
6	1290
7	1310
8	1330

5. Recommended Power Supply Filter

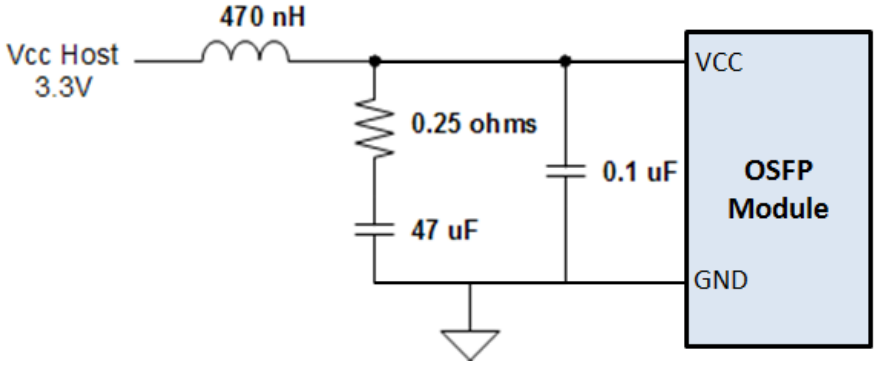

Figure 4. Recommended Power Supply Filter

6. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	15	70	degC	
Power Supply Voltage	V_{CC}	-0.3	3.6	V	
Power Dissipation			16	W	
Relative Humidity (non-condensation)	RH	5	85	%	

7. Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			106.25		Gbps	
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.0x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance with G.652	D	2		3000	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

8. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				16	W	400G,FEC bypass mode
				12		200G Mode
Supply Current	Icc			4.84	A	400G
				3.63		200G
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	53.125 ± 100 ppm			GBd	
DC Common-mode input Voltage	TP1	-0.3		2.8	V	
Single-ended input Voltage	TP1a	-0.4		3.3	V	
AC Common-mode RMS input Voltage	TP1a			17.5	mV	
Module stressed input test		IEEE 802.3ck 120G3.4.1				
Differential Peak-to-Peak input Voltage	TP1a			900	mV	
Differential input Eye Height	TP1a	15			mV	
Differential input Vertical Eye Closure	TP1a	9		9.5	dB	
Common to Different Mode input Return Loss	TP1	IEEE802.3ck Equation 120G-1				
Effective input Return Loss	TP1		TBD		dB	
Differential input Termination Mismatch	TP1			10	%	
Input Transition time (20% to 80%)	TP1a	7.5			ps	
Receiver (each Lane)						
Signaling Rate, each lane	TP4	53.125 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mV	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	

Differential Termination Mismatch	TP4			10	%	
Differential Near-end output Eye Height	TP4	24			mV	

Near-end vertical eye closure				7.5	dB	
Differential Far-end output Eye Height	TP4	24			mV	
Far-end vertical eye closure	TP4			7.5	dB	
Common-mode to Differential mode output Return Loss	TP4	IEEE802.3ck Equation 120G-1			dB	
Effective output Return Loss	TP4		TBD		dB	
Output Transition time (20% to 80%)	TP4	7.5			ps	
DC Common-mode output Voltage	TP4	-350		2850	mV	

9. Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Wavelength Assignment	L0	1265.25	1271	1276.75	nm	
	L1	1285.25	1291	1296.75	nm	
	L2	1305.25	1311	1316.75	nm	
	L3	1325.25	1331	1336.75	nm	
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P_T			9.5	dBm	
Average Launch Power, each Lane	P_{AVG}	-3.2		3.5	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	max(-0.2,-1.6+TDECQ)		3.7	dBm	2
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
Transmitter eye Closure for PAM4, each Lane	TECQ			3.4	dB	

|TDECQ-TECQ|				2.5	dB	
Over/under-shoot				22	%	

Transmitter power excursion				1.8	dBm	
Extinction Ratio	ER	3.5			dB	
Difference in Launch Power between any Two Lanes (OMA_{outer})				4.0	dB	
$RIN_{17.1}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			17.1	dB	
Transmitter Reflectance	R_T			-26	dB	
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-16	dBm	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	TH_d	5.7			dBm	3
Average Receive Power, each Lane		-7.2		3.5	dBm	4
Receive Power (OMA_{outer}), each Lane				3.7	dBm	
Difference in Receiver Power between any Two Lanes (OMA_{outer})				4.1	Db	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			Equation (1)	dBm	5
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-2.6	dBm	6

Receiver Reflectance	R_R			-26	Db	
Bit error ratio floor	BER_FL			3.4E-6		7
LOS Assert	LOSA	-20			dBm	
LOS De-assert	LOSD			-10.3	dBm	

LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 8)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		3.4			dB	
OMA_{outer} of each Aggressor Lane		1.4			dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. The values for OMA_{outer} each lane (min) vary with TDECQ. The relationships are illustrated in Figure 5 along with the values for OMA_{outer} each lane (max).
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of TECQ up to 3.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 5.

$$RS = \max(-4.6,\ TECQ - 6.0)\ dBm \quad (1)$$

Where:

RS is the receiver sensitivity, and

TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.

6. Measured with conformance test signal at TP3 for the BER equal to $2.4x10^{-4}$.
7. Measured with a reference transmitter to produce SECQ greater than or equal to 2dB. The BER at receiver must stay within the specified limit over an OMA range of (-4.9 + TDECQ) dBm to 3.7dBm.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

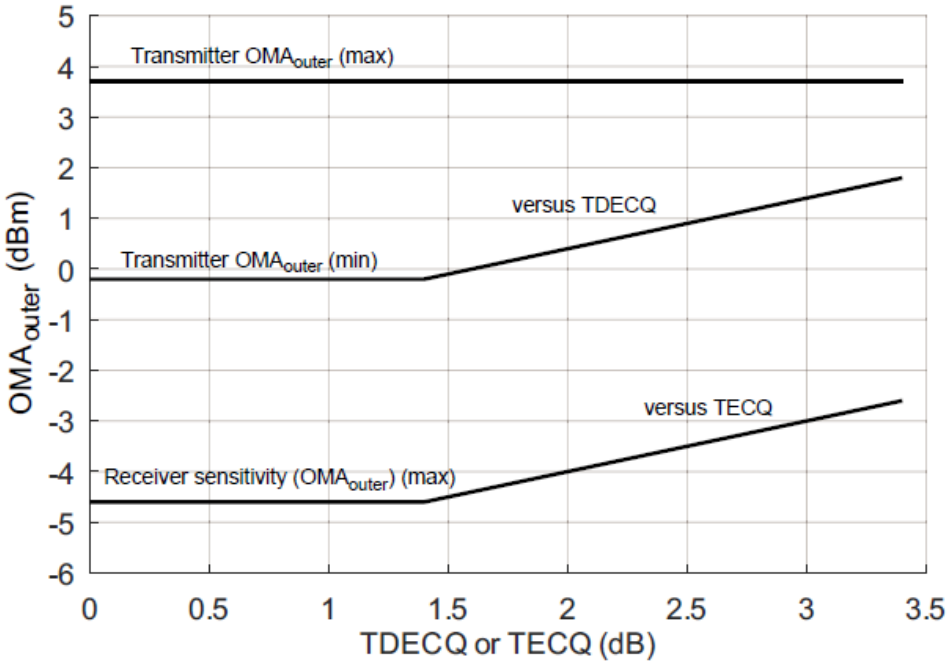

Figure 5. Illustration of Transmitter OMA_{outer} and Receiver Sensitivity Mask for 2x400G-FR4

10. Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range

Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

11. Mechanical Dimensions

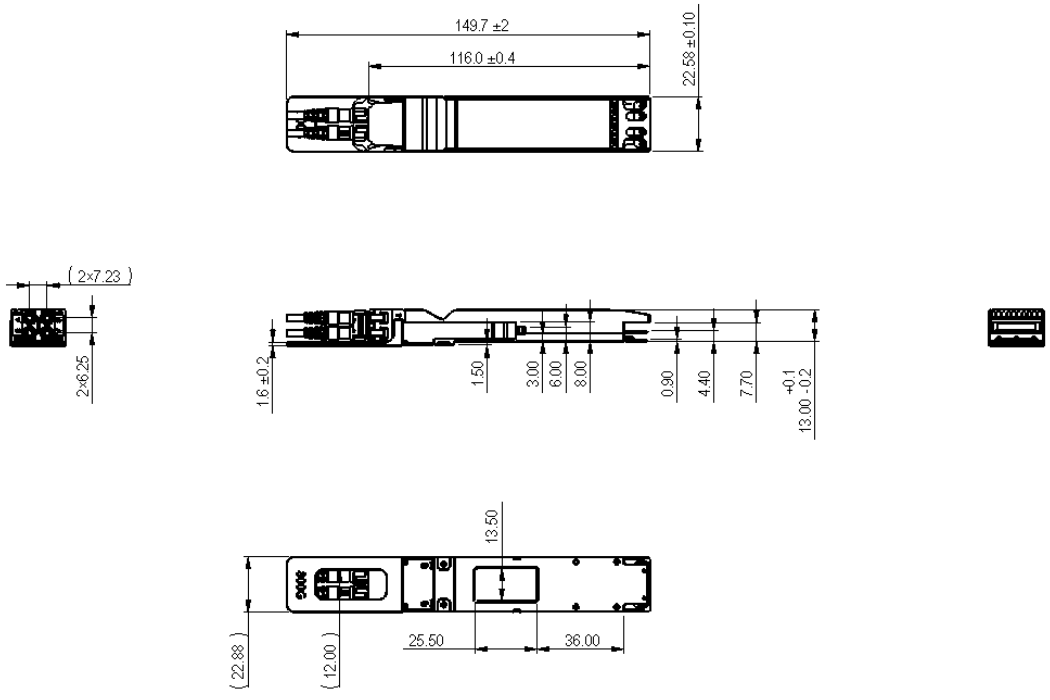

Figure 6. Mechanical Outline

12. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

13. Laser Safety

This is a Class I Laser Product, or Class 1 Laser Product according to IEC/EN 60825-1:2014.

This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

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